L Number	Hits	Search Text	DB	Time stamp
31	110	check near3 swap$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 19:43
32	0	(check near3 swap$4) same vaild	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 19:44
33	3	(check near3 swap$4) same valid	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:53
34	2	("20030046505").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:18
35	2	("6658522").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:18
36	0	(5987565.PN. and ((network same (swap$4 near3 memory)) and @ay<2002)) and "252"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:18
37	1	(("6658522").PN.) and "252"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:18
38	0	swap$4 near2 meeory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:54
39	1473	swap$4 near2 memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:54
40	3	(swap$4 near2 memory) same (valid near2 bit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:58
41	123	swap$4 same (valid near2 bit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:58
42	46	(swap$4 same (valid near2 bit)) same table	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 20:59
-	2	("20030046505").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 20:07
-	1380	swap$4 same zero	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 20:07

-	339	(swap$4 same zero) same memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 21:47
-	1	((swap$4 same zero) same memory) and vaild	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 21:46
-	6036	swap$4 same memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 21:47
-	9922	(swap$4 same memory) sane quiesce	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 21:47
-	3	(swap$4 same memory) same quiesce	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 21:57
-	2	("20020091841").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 22:12
-	2	("20030046490").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/20 22:18
-	2	("20030046497").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 11:03
-	43	network same swap$4 same valid	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 11:06
-	0	san same swap$4 same valid	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 11:06
-	39	san same swap$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 19:43
-	194	network same (swap$4 near3 memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 11:16
-	167	(network same (swap$4 near3 memory)) and @ay<2002	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/21 11:16

US-PAT-NO: 5388242

DOCUMENT-IDENTIFIER: US 5388242 A

TITLE: Multiprocessor system with each processor executing the same instruction sequence and hierarchical memory providing on demand page swapping

DATE-ISSUED: February 7, 1995

US-CL-CURRENT: 711/113, 711/121 , 711/147 , 711/159 , 711/209

APPL-NO: 07/ 982074

DATE FILED: November 24, 1992

PARENT-CASE:

RELATED CASES

This application is a continuation of copending application Ser. No. 07/282,469 filed on Dec. 9, 1988 now abandoned which discloses subject matter also disclosed in copending application Ser. Nos. 282,538, 282,540, 282,629, 283,139 and 283,141, all abandoned, filed Dec. 9, 1988, and Ser. No. 283,573 and 283,573 now U.S. Pat. No. 4,965,71 and Ser. No. 283,574 filed Dec. 13, 1988 and assigned to Tandem Computers Incorporated.

——— KWIC ———

Detailed Description Text - DETX (98):

If a memory reference is made and a TLB miss is shown, but the page table lookup resulting from the TLB miss exception shows the page is in local memory, then a TLB entry is made to show this page to be in local memory. That is, the process takes an exception when the TLB miss occurs, goes to the page tables (in the kernel data section), finds the table entry, writes to TLB, then the process is allowed to proceed. But if the memory reference shows a TLB miss, and the page tables show the corresponding physical address is in global memory (over 8M physical address), the TLB entry is made for this page, and when the process resumes it will find the page entry in the TLB as before; yet another exception is taken because the valid bit will be zero, indicating the page is physically not in local memory, so this time the exception will enter a routine to swap the page from global to local and validate the TLB entry, so execution can then proceed. In the third situation, if the page tables show address for the memory reference is on disk, not in local or global memory, then the system operates as indicated above, i.e., the process is put off the run queue and put in the sleep queue, a disk request is made, and when the disk has transferred the page to global memory and signalled a command-complete interrupt, then the page is swapped from global to local, and the TLB updated, then the process can execute again.

PGPUB-DOCUMENT-NUMBER: 20010025315

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010025315 A1

TITLE: Term addressable memory of an accelerator system and method

PUBLICATION-DATE: September 27, 2001

US-CL-CURRENT: 709/231

APPL-NO: 09/ 756667

DATE FILED: January 10, 2001

RELATED-US-APPL-DATA:

child 09756667 A1 20010110

parent continuation-in-part-of 09147856 19990517 US GRANTED

parent-patent 6173333 US

——— KWIC ———

Pre-Grant Publication Document Identifier - DID (1):
US 20010025315 A1

Application Filing Year - APY (1):
2001

Detail Description Paragraph - DETX (21):
[0045] The memory 24 will contain the host system view of network memory, and a shadowed copy for the network accelerator to use for TCP segment transmission and reception. The host system software driver will swap application memory (system RAM) for memory 24. This will allow the host system direct access the network data stored in the dual-port/double banked memory, effectively replacing the role of host system RAM. Finally, the system interface controls the relationship between the system and the network accelerator. It contains configuration and status registers, and allows the host system to access the network accelerator.

PGPUB-DOCUMENT-NUMBER: 20020144073

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020144073 A1

TITLE: Method for memory heap and buddy system management for service aware networks

PUBLICATION-DATE: October 3, 2002

US-CL-CURRENT: 711/170

APPL-NO: 09/ 824970

DATE FILED: April 3, 2001

——— KWIC ———

Summary of Invention Paragraph - BSTX (4):

[0002] Memory management systems for processing units handling multiple tasks are required to handle the memory needs of each task as they are swapped in and out of memory. The different tasks may require various sizes of memory space during various times of their execution period. Hence, memory needs are dynamic and may grow or shrink over time. In addition, when the task is complete, the memory associated with its execution may be freed to be used by other tasks, which may require that additional memory be made available. A specific use of heap memories may be found in service aware networks (hereinafter "SAN") where a task may handle multiple process flows and require varying sizes of memory to handle the task.

US-PAT-NO: 5890003

DOCUMENT-IDENTIFIER: US 5890003 A

TITLE: Interrupts between asynchronously operating CPUs in fault tolerant computer system

DATE-ISSUED: March 30, 1999

US-CL-CURRENT: 710/263, 712/244 , 714/11

APPL-NO: 08/ 116950

DATE FILED: September 7, 1993

PARENT-CASE:

This application is a continuation of Ser. No. 07/517,533 filed Apr. 25, 1990, now abandoned, which is a continuation of Ser. No. 07/282,538 filed Dec. 9, 1988, now abandoned.

——— KWIC ———

Detailed Description Text - DETX (98):

If a memory reference is made and a TLB miss is shown, but the page table lookup resulting from the TLB miss exception shows the page is in local memory, then a TLB entry is made to show this page to be in local memory. That is, the process takes an exception when the TLB miss occurs, goes to the page tables (in the kernel data section), finds the table entry, writes to TLB, then the process is allowed to proceed. But if the memory reference shows a TLB miss, and the page tables show the corresponding physical address is in global memory (over 8M physical address), the TLB entry is made for this page, and when the process resumes it will find the page entry in the TLB as before; yet another exception is taken because the valid bit will be zero, indicating the page is physically not in local memory, so this time the exception will enter a routine to swap the page from global to local and validate the TLB entry, so execution can then proceed. In the third situation, if the page tables show address for the memory reference is on disk, not in local or global memory, then the system operates as indicated above, i.e., the process is put off the run queue and put in the sleep queue, a disk request is made, and when the disk has transferred the page to global memory and signalled a command-complete interrupt, then the page is swapped from global to local, and the TLB updated, then the process can execute again.